Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1. (Original) A method of forming a fin field effect transistor, comprising:

 forming a mesa on a silicon-on-insulator wafer;

 forming a dummy gate with a first material in a first pattern over the mesa;

 forming a first dielectric layer around the dummy gate;

 removing the first material to create a trench shaped in the first pattern;

 forming a mask over a portion of the trench and the mesa;

 etching a portion of the mesa that is exposed within the trench to form a fin;

 forming a gate dielectric layer over the fin;

 forming a gate within the trench over the gate dielectric layer; and

 removing the first dielectric layer.
- 2. (Original) The method of claim 1, wherein the gate contacts at least three surfaces of the fin.
- 3. (Original) The method of claim 2, wherein the fin field effect transistor comprises a trigate fin field effect transistor.
- 4. (Original) The method of claim 1, wherein the first dielectric layer comprises tetraethylorthosilicate (TEOS).

- 5. (Original) The method of claim 1, wherein the gate dielectric layer comprises at least one of SiO, SiO₂, SiN, SiON, HFO₂, ZrO₂, Al₂O₃, HfSiO(x) and HfSiO(x)N(1-x).
- 6. (Original) The method of claim 1, wherein the first material comprises Si₃N₄.
- 7. (Original) The method of claim 1, further comprising:
 forming a layer of sacrificial oxide over the fin; and
 removing the sacrificial oxide, prior to forming the gate, to remove defects from
 sidewalls of the fin.
- 8. (Original) The method of claim 1, wherein forming the gate comprises: depositing polysilicon within the trench; and polishing the polysilicon to an upper surface of the first dielectric layer to planarize the polysilicon.
- 9. (Original) The method of claim 1, wherein the fin has a rectangular cross-section with a width ranging from about 15 nm to about 30 nm.
- 10. (Original) The method of claim 1, wherein the mesa comprises a silicon layer and an oxide layer formed over the silicon layer.

- 11. (Original) The method of claim 10, wherein a thickness of the silicon layer ranges from about 10 nm to about 50 nm.
- 12. (Original) The method of claim 11, wherein a thickness of the oxide layer ranges from about 10 nm to about 15 nm.
- 13. (Original) The method of claim 1, wherein a thickness of the gate in a channel region of the fin field effect transistor ranges from about 80 nm to about 120 nm.
- 14. (Original) The method of claim 1, wherein the silicon-on-insulator wafer is fully depleted and forming the mesa comprises:

forming a silicon layer;

forming a silicon dioxide layer over the silicon layer; and etching the silicon and silicon dioxide layers using a rectangular mask to isolate the mesa.

15. (Currently amended) A method of forming a tri-gate fin field effect transistor, comprising:

forming an oxide layer over a silicon-on-insulator wafer comprising a silicon layer; etching the silicon and oxide layers using a rectangular mask to form a mesa; etching a portion of the mesa using a second mask to form a fin, wherein the etching a

portion of the mesa includes:

etching a portion of the mesa in a channel region of the tri-gate fin field effect transistor;

forming a gate dielectric layer over the fin; and forming a tri-gate over the fin and the gate dielectric layer.

- 16. (Original) The method of claim 15, wherein a thickness of the silicon layer ranges from about 10 nm to about 50 nm.
- 17. (Original) The method of claim 15, wherein a thickness of the oxide layer ranges from about 10 nm to about 15 nm.
- 18. (Original) The method of claim 15, wherein a thickness of the tri-gate in a channel region of the fin field effect transistor ranges from about 80 nm to about 120 nm.
- 19. (Canceled)
- 20. (Currently amended) The method of claim <u>15</u> 19, wherein a width of the fin in the channel region ranges from about 15 nm to about 30 nm.